

EntropyDFT™ Test Point & Scan Insertion Tool *Product Fact Sheet*

U.S. Patent Application # 18/377,095 and U.S. Patent # 8,164,345

EntropyDFT™ Overview

EntropyDFT™ inserts test hardware into a logic circuit in the form of scannable flip-flops, latches, test points, and/or multiplexers, such that the design has better device controllability and observability.

The tool fits into the standard *Design-for-Testability* (DFT) work flow between logic synthesis and *Automatic Test-Pattern Generation* (ATPG). It typically reduces TV (*Test Data Volume*) by **50 to 64%** and can improve test coverage by over **10.0%** on huge circuits. Recently, the tool added **0.71%** chip area for test points; commercial tools add **4%**. *EntropyDFT™* also significantly reduces ATPG run time. It provides a report of stuck-at fault loss (both uncontrollable and unobservable) due to each problem signal. Signals in the report are sorted in decreasing order by the fault loss they cause. Optionally, they can be sorted by the fraction of the time the signal is **X/Z**, and within that by the fault loss. *EntropyDFT™* typically runs in 1 hour.

EntropyDFT™ is a unique, standalone tool that employs patented technology to enhance **existing DFT and ATPG flows** while offering significant test coverage and test time benefits. It dramatically reduces the time needed to find the causes and fixes for X's in a design. It has the fault loss features of the *EntropyXZ™* tool, and also can insert and optimize test points into the circuit.

EntropyDFT™ Target Users

Back-end IC designers who are DFT engineers use *EntropyDFT™*. Front-end designers may also use it to specify design sections that must not be altered. A verification engineer might use it to obtain diagnostics for verification and debug.

EntropyDFT™ Features

EntropyDFT identifies signals in a design where ATPG test coverage will be improved by making that signal an accessible *test point* (TP), and inserts scannable flip-flops, latches, test points, and/or multiplexers in the

design's gate-level netlist. It works on a netlist that already implements full scan or it can implement either full or partial scan on its own. The tool automatically chooses test point locations and types.

The inserted test point¹ will be one of five types:

<i>control-to-0</i>	Force an internal signal to 0
<i>control-to-1</i>	Force an internal signal to 1
<i>observe_only</i>	No force; observe only
<i>complete</i>	Force 0 or 1, as well as observe
<i>blocker</i>	Replaces an X/Z signal with 0 or 1

EntropyDFT™ Technology

EntropyDFT™ uses a testability measure called *entropy*, or information flow. Claude Shannon invented this information measure in the 1940's when he created the field of *information theory*, which revolutionized communications systems. Shannon's *entropy* is extraordinarily effective as a large circuit testability measure, and greatly improves DFT/ATPG effectiveness in commercial *Electronic Design Automation* (EDA) tools.

The entropy, *E*, of a logic signal is:

$$E = -p(0) \log_2(p(0)) - p(1) \log_2(p(1))$$

where *p*(0) is the probability of the signal being 0, and *p*(1) is the probability of it being a 1. A signal's entropy is maximized to 1.0 when both logic 0 and logic 1 have equal probabilities of 0.5. If one or the other of the two logic values cannot be obtained at a point in the circuit, then its entropy is 0. Intermediate signal probabilities lead to intermediate *E* values.

EntropyDFT™ uses an extremely fast internal logic simulator that determines the device entropies based on a controlled set of vectors that exercises the gate level netlist. The user controls the hardware overhead and has limited control of the vectors. The tool chooses optimal candidates for scanning and test points based on *E* and other testability measures. Entropy also uses the digital frequency response of signals for a testability measure.

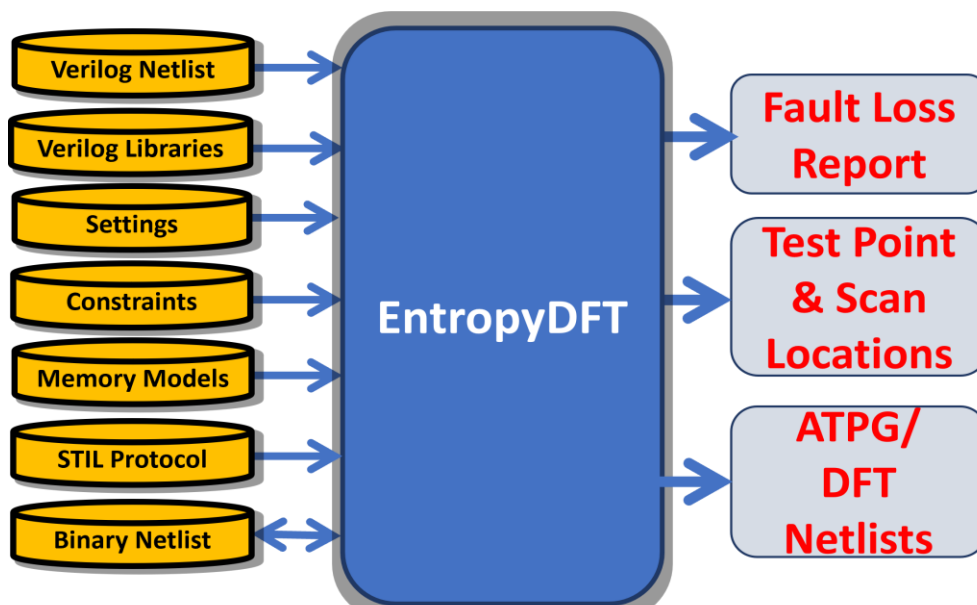


Figure 1: EntropyDFT™ Inputs and Outputs

Integrating EntropyDFT™ into an Existing ATPG Flow

In a typical *System-on-a-Chip* (SoC) development flow, DFT starts at the front-end configuration of scan chains in RTL design descriptions. With synthesis and other applications (such as test rule check, etc.), front-end DFT produces a flattened netlist that passed all design, scan, and test rule checks. *EntropyDFT™* integrates non-disruptively with the DFT and ATPG solutions from Siemens™, Cadence™, and Synopsys™.

Figure 1 shows the *EntropyDFT™* dataflow. The tool runs on the Redhat Linux O/S.

EntropyDFT™ Results on Benchmarks

ATPG Results for 6 Large Circuits

Ckt	# Gates no FFs or Latches	Test Coverage (%)		Vector Length		Added Transistors (%)	Layout Area Increase (%)
		No DFT	+ TPs	No DFT	+ TPs		
b14	4444	99.74	99.99	395	345	0.999	0.903
b15	8338	98.67	99.96	462	455	1.006	0.628
b17	22645	99.34	99.99	503	478	0.999	0.629
b20	8875	99.87	99.99	456	411	0.997	0.845
b21	9259	99.82	99.99	438	412	0.995	0.824
b22	14282	99.87	99.98	456	402	1.002	0.672
Ave	11316	99.55	99.98	452	417	1.000	0.708

On these examples, Entropy reduced CPU time for ATPG by **62.97%**. It increased test coverage by **0.43%**, reduced vector length by **7.638%**, and its average chip area increase for test points was **0.71%**.

On huge cell phone chips, *EntropyDFT™*:

- Improved stuck-fault test cov. by up to **13.60%**.
- Reduced stuck-fault test count by up to **26.83%**.
- Improved transition test cov. by up to **23.99%**.
- Reduced transition test count by up to **77.23%**.

On a microprocessor, it recovered 1431 lost faults with only 7 test points (<< 0.5% overhead).

These numbers indicate a huge reduction in error and test cost, beyond what test data compression can do.

About Spectral Chip Test Research LLC

Spectral is a Semiconductor Point Solution provider targeting systems and semiconductor organizations seeking productivity improvement. We solve ASIC test problems with in-house domain experts. We offer solutions and specialized services for DFT.

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1. Test points are essential for acceptable circuit test coverage by either built-in self-testing or external testing. They control internal signals to logic 0 or 1, or they observe signals. They are activated by input test control signals.